Appendix: Amended Claims in Marked-Up Form

42. (Amended) A computer system, comprising:

a bus;

a central processing unit coupled to said bus; and

a graphics accelerator coupled to said bus, said graphics accelerator including a texture cache system, said texture cache system including a texture cache memory that stores texels to be used by a texel value generating circuit, a cache controller that controls said texture cache memory in accordance with a [replacement control component that implements a] replacement policy [for said texture cache memory], and a direct memory access engine that retrieves texel data from memory.

52. (Amended) A texture mapping method using a [texture cache system, said texture cache system] graphics accelerator, said graphics accelerator including a texture cache memory, a [replacement control component] cache controller that controls the texture cache memory in accordance with a cache replacement policy, and a direct memory access engine, comprising:

(a) retrieving texels from memory via the direct memory access engine;

(b) storing said retrieved texels in the texture cache memory in accordance with a replacement policy that is determined by the [replacement control component] cache controller; and

(c) rendering a polygon using texels that are stored in the texture cache memory.

56. (Amended) The texture mapping method of claim 55, wherein said storing comprises reviewing a state of flags within at least one set of flags that are associated with cache lines of said texture cache memory.

62. (Amended) A computer system, comprising:

a memory; and

a memory control that stores two-dimensional data in said memory, wherein said data is stored in said memory using an interleaved address that is formed by interleaving individual bit values of a coordinate in a first dimension with individual bit values of a coordinate in a second dimension, wherein at least part of said interleaved address has a bit pattern that includes multiple bit values of said first dimension coordinate at odd-numbered bit positions and multiple bit values of said second dimension coordinate at even-numbered bit positions.

66. (Amended) A texture caching method, comprising:

(a) identifying a set of two-dimensional data that is to be transferred into memory; and

(b) storing said set of two-dimensional data in memory using an interleaved address that is formed by interleaving individual bit values of a coordinate in a first dimension with individual bit values of a coordinate in a second dimension, wherein at least part of said interleaved address has a bit pattern that includes multiple bit values of

said first dimension coordinate at odd-numbered bit positions and multiple bit values of said second dimension coordinate at even-numbered bit positions.

69. (Amended) The method of claim 68, wherein said storing comprises storing texels in linear cache lines of [said] a texture cache in said graphics accelerator.